

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Wing K. Luk
Robert H. Dennard

Docket No.: YOR920030603US1

Serial No.: Unassigned

Filing Date: Concurrently Herewith

Title: **AMPLIFIERS USING GATED DIODES**

INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following document(s) listed on the accompanying PTO Form 1449.

Copies of each of the following listed items are enclosed:

Other Documents

1. Allen et al., "CMOS Analog Circuit Design," pg. 469 (1987).

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability or that no other material information exists.

Respectfully submitted,



Robert J. Mauri
Attorney for Applicants
Reg. No. 41,180
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560

Date: January 5, 2004

Applicant: Wing K. Luk
Robert H. Dennard
Docket No.: YOR920030603US1
Serial No.: Unassigned
Filing Date: Concurrently Herewith
Group: Unassigned

**LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT**

U.S. PATENT DOCUMENTS

EXAMINER					FILING DATE
INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER					TRANSLATION	
INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	YES	NO

OTHER DOCUMENTS

EXAMINER			
INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.	

_____ Allen et al., "CMOS Analog Circuit Design," pg. 469 (1987).

Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.